



# AZ100LVEL16VT ARIZONA MICROTEK, INC.

## ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

### FEATURES

- High Bandwidth for  $\geq 1\text{GHz}$
- **Similar Operation as AZ100LVEL16VR except in Disabled Condition:  $Q_{HG}$  is High**
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a 3x3 mm or 2x2 mm MLP Package
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website

### PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNA+	P9+ <Date Code>	1,2
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNB+	P8+ <Date Code>	1,2
MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTL+	AZM+ 16T <Date Code>	1,2

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.

### DESCRIPTION

The AZ100LVEL16VT is a specialized oscillator gain stage with high gain output buffer including an enable. The  $Q_{HG}/Q_{HG}$  outputs have a voltage gain several times greater than the Q/Q outputs.

#### MLP 16, 3x3 mm Package (VTL)

The AZ100LVEL16VTL and provide a selectable enable input (EN) that allows continuous oscillator operation. See truth table for the Enable function. If Enable pull-up is desired in the CMOS/TTL mode, an external  $\leq 20\text{k}\Omega$  resistor connecting EN to  $V_{CC}$  will override the on-chip pull-down resistor. When disabled, the  $Q_{HG}$  output is forced high and the  $Q_{HG}$  output is forced low. The AZ100LVEL16VTL also provides a  $V_{BB}$  and  $470\Omega$  internal bias resistors from D to  $V_{BB}$  and  $D$  to  $V_{BB}$ . The  $V_{BB}$  pin can support 1.5mA sink/source current. Bypassing  $V_{BB}$  to ground with a  $0.01\ \mu\text{F}$  capacitor is recommended.

The outputs Q and Q each have a selectable on-chip pull-down current source. See truth table below for current source functions. External resistors may also be used to increase pull-down current to a maximum total of 25mA.

Outputs  $Q_{HG}$  and  $Q_{HG}$  each have an optional on-chip pull-down current source of 10mA. When pad/pin  $V_{EEP}$  is left open (NC), the output current sources are disabled and the  $Q_{HG}/Q_{HG}$  operate as standard PECL/ECL. When  $V_{EEP}$  is connected to  $V_{EE}$ , the current sources are activated. The  $Q_{HG}/Q_{HG}$  pull-down current can be decreased, by using a resistor to connect  $V_{EEP}$  to  $V_{EE}$ . (See graph on page 5.)

#### MLP 8, 2x2 mm Package, VTNA & VTNB Versions

All MLP 8, 2x2mm versions of the AZ100LVEL16VT provide an enable input that allows continuous oscillator operation. VTNA and VTNB utilize an enable (EN) that operates in the PECL/ECL mode. When the EN input is LOW, the Q and  $Q_{HG}/Q_{HG}$  outputs follow the data inputs. When EN is HIGH, the  $Q_{HG}$  output is forced high and the  $Q_{HG}$  output is forced low.

For VTNA, both D and D inputs are brought out and tied to the  $V_{BB}$  pin through  $470\Omega$  internal bias resistors. In the VTNB, the D input is internally tied directly to the  $V_{BB}$  pin and the D input is tied to the  $V_{BB}$  pin through a  $470\Omega$  internal bias resistor. Bypassing  $V_{BB}$  to ground with a  $0.01\ \mu\text{F}$  capacitor is recommended.

All MLP 8, 2x2mm versions (VTNA & VTNB) have the Q,  $Q_{HG}$ , and  $Q_{HG}$  current sources disabled, while the Q output operates with a 4mA current source to  $V_{EE}$ .

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

# AZ100LVEL16VT

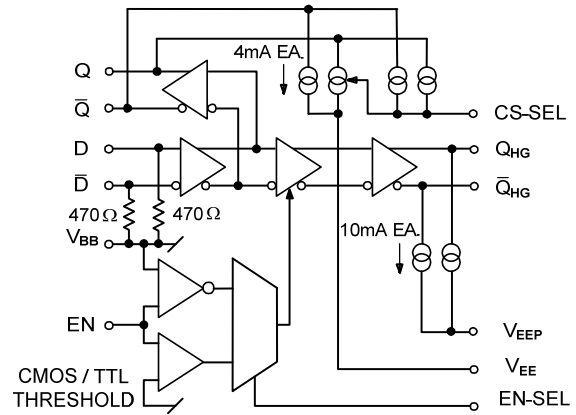
**ENABLE TRUTH TABLE  
MLP 16 (VTL)**

EN-SEL	EN	Q/Q	Q <sub>HG</sub>	Q <sub>HG</sub>
NC	PECL Low, V <sub>EE</sub> or NC	Data	Data	Data
NC	PECL High or V <sub>CC</sub>	Data	High	Low
V <sub>EE</sub> *	CMOS Low or V <sub>EE</sub>	Data	High	Low
V <sub>EE</sub> *	CMOS High or V <sub>CC</sub>	Data	Data	Data
V <sub>EE</sub> *	NC, no external pull-up	Data	High	Low
V <sub>EE</sub> *	NC, with ≤20kΩ to V <sub>CC</sub>	Data	Data	Data

\*Connections to V<sub>CC</sub> or V<sub>EE</sub> must be less than 1Ω.

## PIN DESCRIPTION

PIN	FUNCTION
D/D	Data Inputs
Q/Q	Data Outputs
Q <sub>HG</sub> /Q <sub>HG</sub>	Data Outputs w/High Gain
V <sub>BB</sub>	Reference Voltage Output
EN-SEL	Selects Enable Logic
EN/EN	Enable Input
CS-SEL	Selects Q and Q Current Source Magnitude
V <sub>EHP</sub>	Optional Q <sub>HG</sub> and Q <sub>HG</sub> Current Sources
V <sub>EE</sub>	Negative Supply
V <sub>CC</sub>	Positive Supply



**MLP 16 (VTL)**

**CURRENT SOURCE TRUTH TABLE  
MLP 16 (VTL)**

CS-SEL	Q	Q
NC	4mA typ.	4mA typ.
V <sub>EE</sub> *	8mA typ.	8mA typ.
V <sub>CC</sub> *	0	4mA typ.

\*Connections to V<sub>CC</sub> or V<sub>EE</sub> must be less than 1Ω.

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
V <sub>CC</sub>	PECL Power Supply (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>D/D</sub>	PECL D/D Input Voltage (V <sub>EE</sub> = 0V)	±0.75 with respect to V <sub>BB</sub>	Vdc
V <sub>EN</sub>	PECL EN Input Voltage (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>EE</sub>	ECL Power Supply (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
V <sub>D/D</sub>	ECL D/D Input Voltage (V <sub>CC</sub> = 0V)	±0.75 with respect to V <sub>BB</sub>	Vdc
V <sub>EN</sub>	ECL EN Input Voltage (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
I <sub>OUT</sub>	Output Current, Q/Q — Continuous — Surge	25 50	mA
I <sub>HGOUT</sub>	Output Current, Q <sub>HG</sub> /Q <sub>HG</sub> — Continuous — Surge	50 100	mA
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

# AZ100LVEL16VT

## 100K ECL DC Characteristics ( $V_{EE} = -3.0V$ to $-5.5V$ , $V_{CC} = GND$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1</sup>	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
$V_{OL}$	Output LOW Voltage <sup>1</sup>	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
$V_{IH}$	Input HIGH Voltage D/D, EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	-1165 $V_{EE}+2000$	-740 $V_{CC}$	-1165 $V_{EE}+2000$	-740 $V_{CC}$	-1165 $V_{EE}+2000$	-740 $V_{CC}$	-1165 $V_{EE}+2000$	-740 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage D/D, EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	-1900 $V_{EE}$	-1475 $V_{EE} + 800$	-1900 $V_{EE}$	-1475 $V_{EE} + 800$	-1900 $V_{EE}$	-1475 $V_{EE} + 800$	-1900 $V_{EE}$	-1475 $V_{EE} + 800$	mV
$V_{BB}$	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN (ECL) <sup>2</sup> EN (CMOS) <sup>3</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		μA
$I_{EE}$	Power Supply Current <sup>1</sup>		48		48		48		54	mA

1.  $Q_{HG}/Q_{HL}$  terminated through 50Ω resistors to  $V_{CC} - 2V$ . VTL also specified with  $V_{EEP}$  and CS-SEL = NC.
2. VTNA, VTNB and VTL with EN-SEL = NC.
3. VTL (only) with EN-SEL =  $V_{CC}$  or  $V_{EE}$ .

## 100K LVPECL DC Characteristics ( $V_{EE} = GND$ , $V_{CC} = +3.3V$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	2255	2465	2275	2465	2275	2465	2275	2465	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	1375	1745	1400	1680	1400	1680	1400	1680	mV
$V_{IH}$	Input HIGH Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	2135 2000	2560 $V_{CC}$	2135 2000	2560 $V_{CC}$	2135 2000	2560 $V_{CC}$	2135 2000	2560 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	1400 GND	1825 800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2.  $Q_{HG}/Q_{HL}$  terminated through 50Ω resistors to  $V_{CC} - 2V$ . VTL also specified with  $V_{EEP}$  and CS-SEL = NC.
3. VTNA, VTNB and VTL with EN-SEL = NC.
4. VTL (only) with EN-SEL =  $V_{CC}$  or  $V_{EE}$ .

## 100K PECL DC Characteristics ( $V_{EE} = GND$ , $V_{CC} = +5.0V$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3955	4165	3975	4165	3975	4165	3975	4165	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3075	3445	3100	3380	3100	3380	3100	3380	mV
$V_{IH}$	Input HIGH Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	3835 2000	4260 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage <sup>1</sup> D/D, EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	3100 GND	3525 800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN (PECL) <sup>3</sup> EN (CMOS) <sup>4</sup>	0.5 -150		0.5 -150		0.5 -150		0.5 -150		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2.  $Q_{HG}/Q_{HL}$  terminated through 50Ω resistors to  $V_{CC} - 2V$ . VTL also specified with  $V_{EEP}$  and CS-SEL = NC.
3. VTNA, VTNB and VTL with EN-SEL = NC.
4. VTL (only) with EN-SEL =  $V_{CC}$  or  $V_{EE}$ .

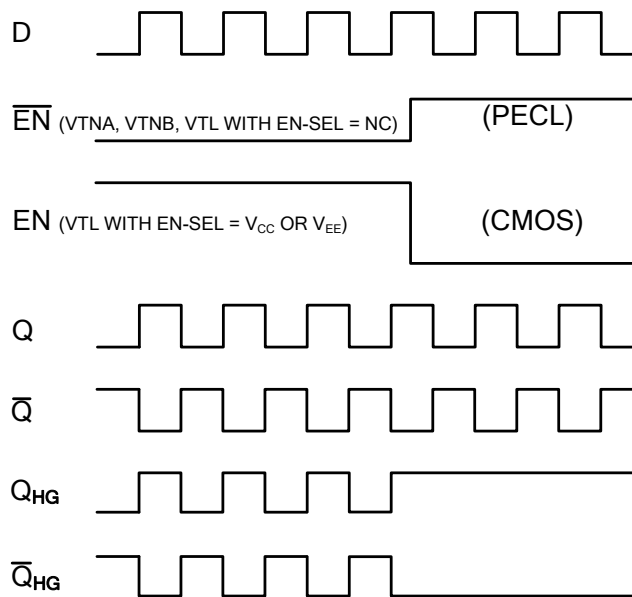
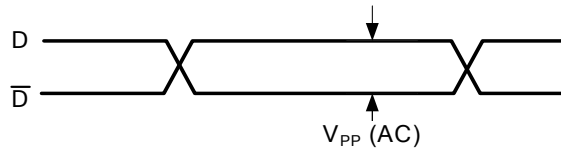
# AZ100LVEL16VT

## AC Characteristics ( $V_{EE} = -3.0V$ to $-5.5V$ ; $V_{CC} = GND$ or $V_{EE} = GND$ ; $V_{CC} = +3.0V$ to $+5.5V$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH} / t_{PHL}$	Propagation Delay D to Q/Q Outputs <sup>1</sup> (SE)			350			350			350			350	ps
	D to $Q_{HG}/\bar{Q}_{HG}$ Outputs <sup>2</sup> (SE)			450			450			450			450	
$t_{SKEW}$	Duty Cycle Skew <sup>3</sup> (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}$	Input Swing <sup>4</sup> Differential (D/D)	80		1000	80		1000	80		1000	80		1000	mV
	Single Ended (D, $\bar{D}$ )	160		1500	160		1500	160		1500	160		1500	
$t_r / t_f$	Output Rise/Fall Times <sup>1,2</sup> (20% - 80%)	100		240	100		240	100		240	100		240	ps

- For VTL, Q/Q outputs specified with an AC coupled 50Ω load and CS-SEL connected to  $V_{EE}$ . For VTNA & VTNB, Q/Q outputs specified with 50Ω termination to  $V_{CC} - 2V$ .
- $Q_{HG}/\bar{Q}_{HG}$  terminated through 50Ω resistors to  $V_{CC} - 2V$ . VTL also specified with  $V_{EEP} = NC$ .
- Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
- The peak-to-peak input swing is the range for which AC parameters are guaranteed. D and  $\bar{D}$  must remain within the range of  $\pm 750$  mV with respect to  $V_{BB}$ . The device has a voltage gain of  $\approx 20$  to the Q/Q outputs and a voltage gain of  $\approx 100$  to the  $Q_{HG}/\bar{Q}_{HG}$  outputs.

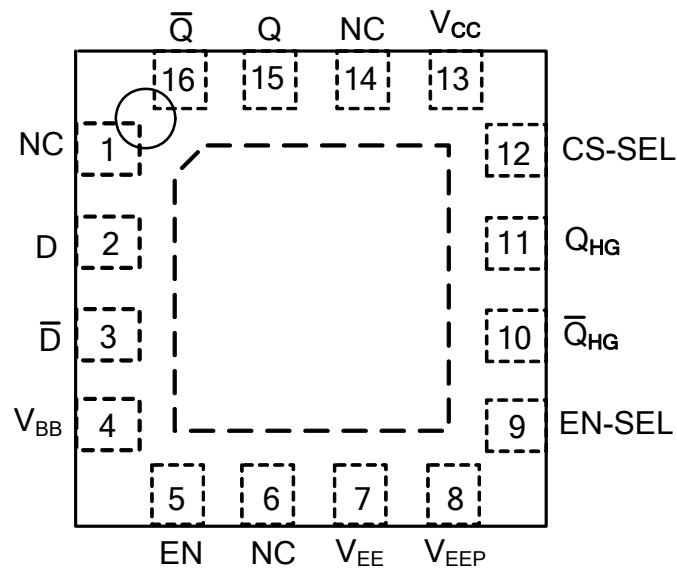
### AC PP INPUT (Differential)



### TIMING DIAGRAM

**AZ100LVEL16VTL**

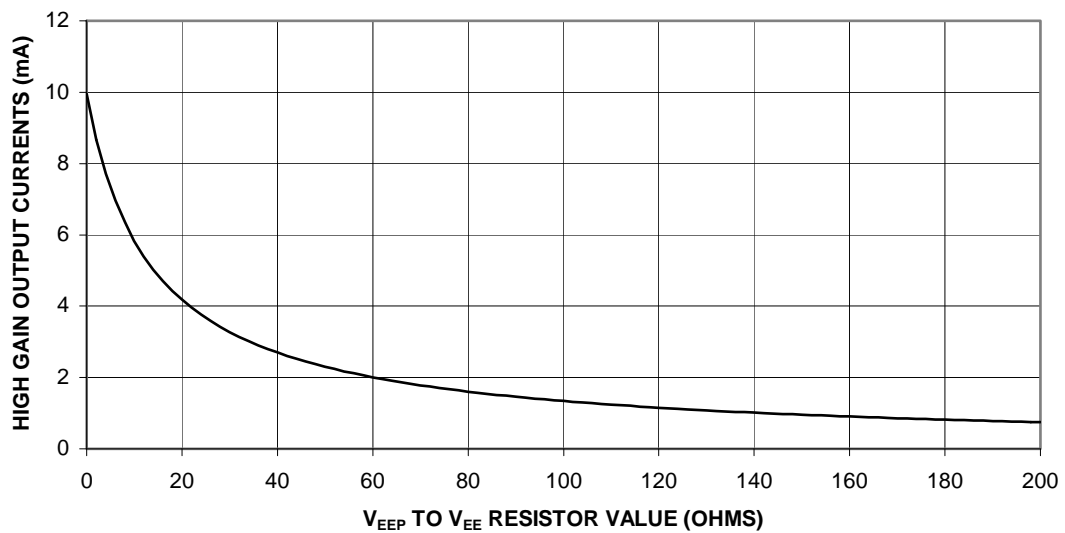
MLP 16  
3x3 mm



TOP VIEW

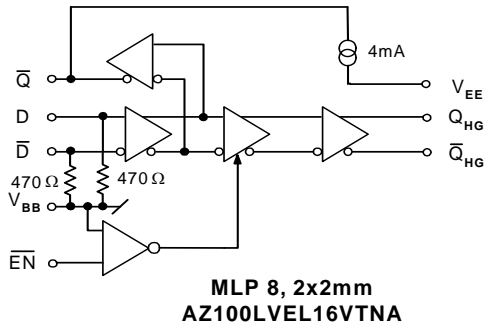
Bottom Center Pad may be left open or tied to V<sub>EE</sub>

**ADJUSTABLE HIGH GAIN OUTPUT CURRENT**

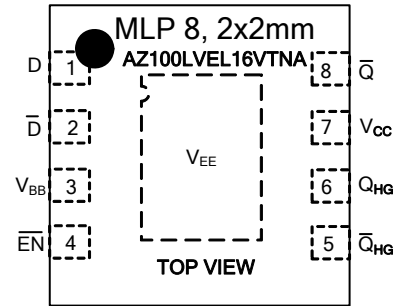


# AZ100LVEL16VT

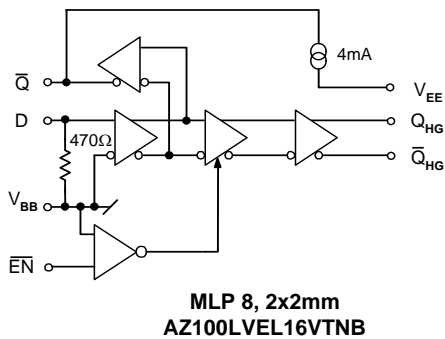
## LOGIC DIAGRAMS AND PINOUTS FOR 2x2mm PACKAGE



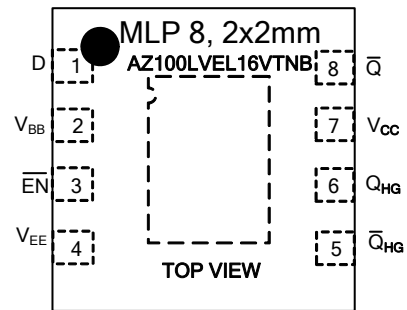
**EN operation follows PECL functionality.  
See Timing Diagram above.**



**Bottom Center Pad is the V<sub>EE</sub> return.**

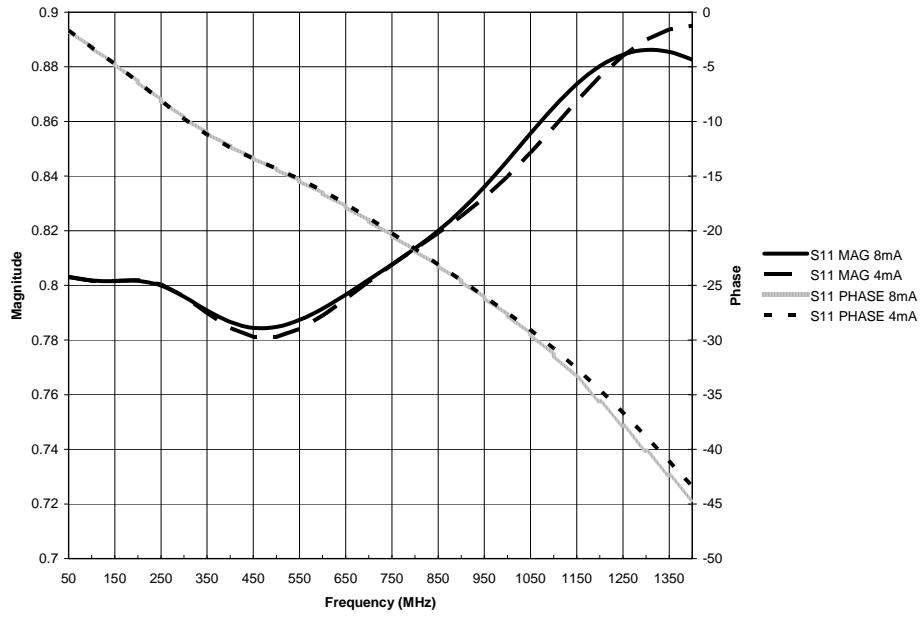


**EN operation follows PECL functionality.  
See Timing Diagram above.**

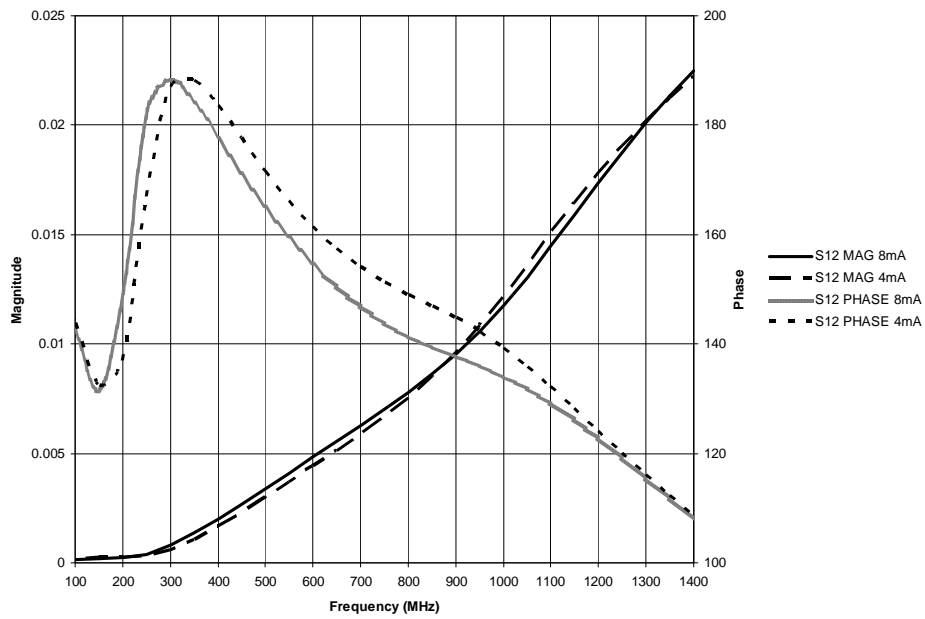


**Bottom Center Pad may be left open  
or tied to V<sub>EE</sub>. Pin 4 is the V<sub>EE</sub> return.**

# AZ100LVEL16VT

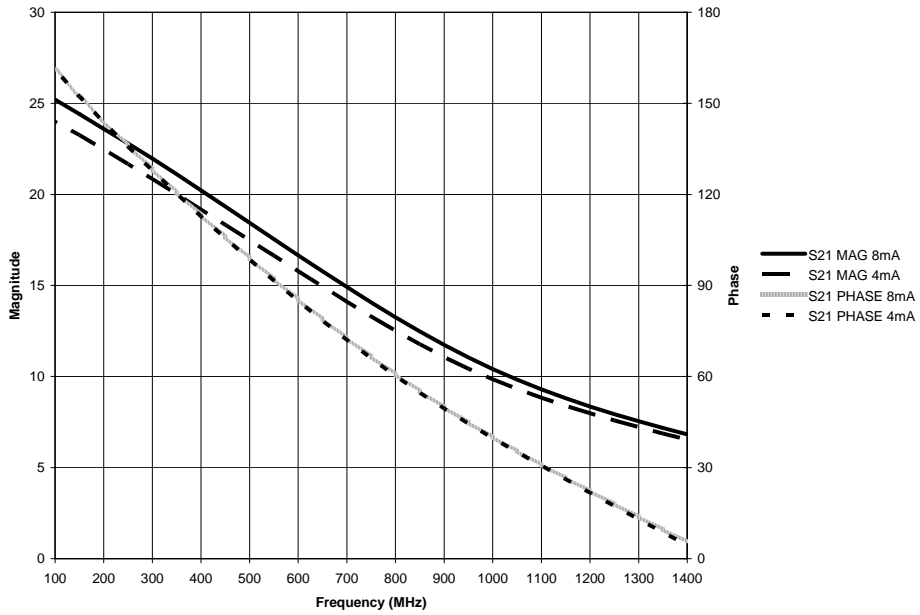


**S11, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

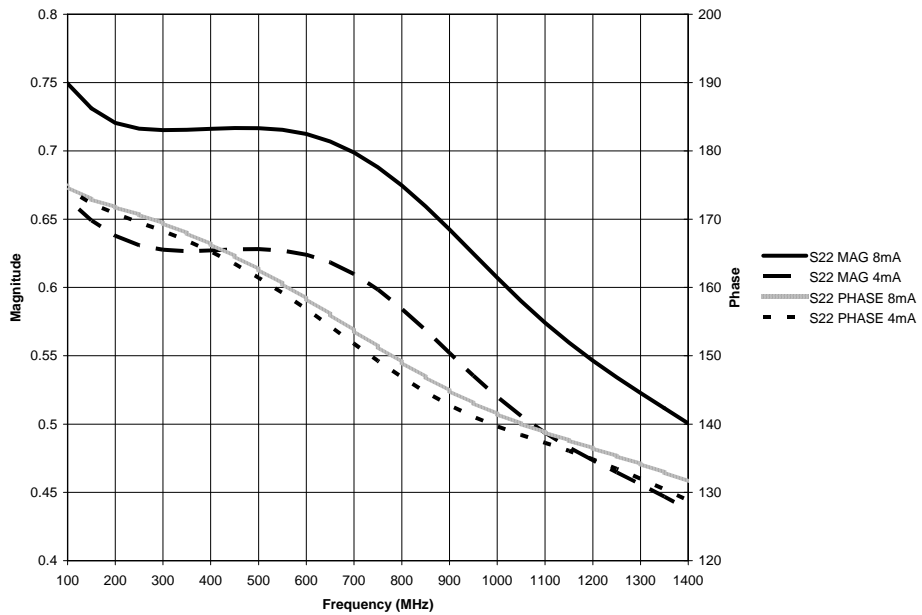


**S12, D to Q**  
(50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

# AZ100LVEL16VT

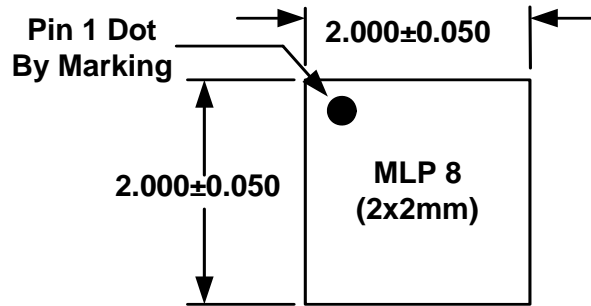


**S21, D to Q**  
 (50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

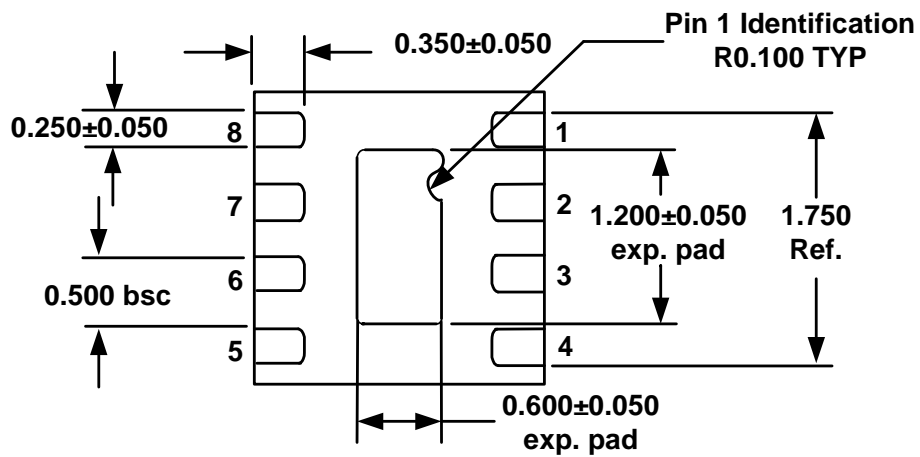


**S22, D to Q**  
 (50  $\Omega$  external AC, 4 & 8mA internal DC Load on Q)

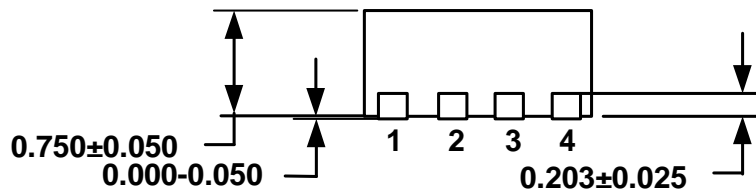
**PACKAGE DIAGRAM**  
**MLP 8 2x2mm**



TOP VIEW



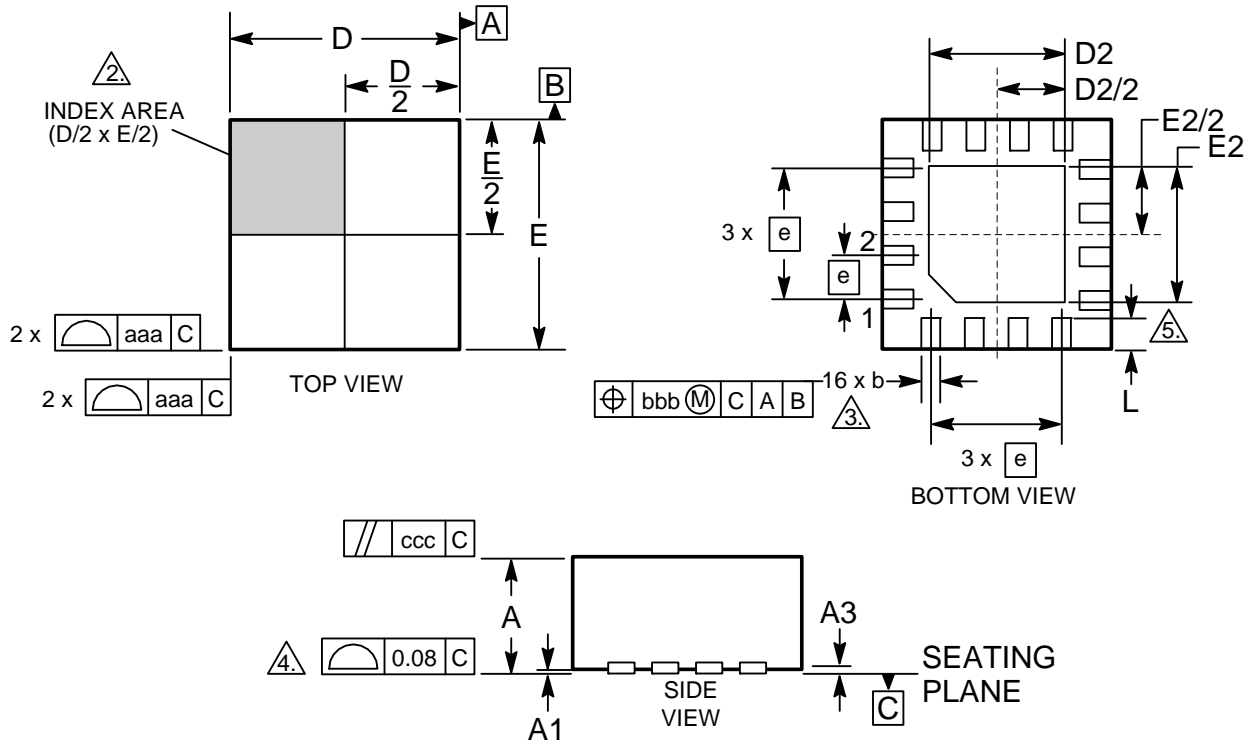
BOTTOM VIEW



SIDE VIEW

**Note: All dimensions are in mm**

**PACKAGE DIAGRAM**  
**MLP 16 3X3mm**



**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
- $\triangle 2$ . THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
- $\triangle 3$ . DIMENSION  $b$  APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
- $\triangle 4$ . COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- $\triangle 5$ . INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

## AZ100LEVEL16VT

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